REMARKS

Reconsideration of this application as amended is respectfully requested.

The Examiner rejected claims 1-19. Claims 1-2 and 18-19 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,954,828 of Lin ("Lin"). Claims 1-6, 12-14, 16, and 18-19 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,182,189 B1 of Alexis ("Alexis"). Claims 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alexis. Claims 15 and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Alexis in view of U.S. Patent publication US 2001/0011318 A1.

Please cancel claim 12-17.

Applicants submit that claim 1 as amended is not anticipated under 35 U.S.C. § 102(b) by Lin. Claim 1 includes the limitations

> a memory array having a first plane, a second plane, a third plane, and a fourth plane, wherein a first partition of the memory array comprises one of the planes and a second partition of the memory array comprises the remaining planes, wherein a write operation is performed on the first partition and a read operation is concurrently performed on the second partition; and
>
> a status register coupled to the memory array, wherein the status register provides status information of the first plane, the second plane, the third plane, and the fourth plane.

(Amended claim 1) (emphasis added).

In contrast, the memory array 10 of Lin includes a fault tolerant section 11 and a header section 12. (Lin, column 4, lines 46-48). Lin does not disclose a memory array having a first plane, a second plane, a third plane and a fourth

plane. Moreover, Lin does not disclose a first partition comprising one of the planes and a second partition comprising the remaining planes, wherein a write operation is performed on the first partition and a read operation is concurrently performed on the second partition. Finally, while Lin discloses **status registers** that include information about each sector of a memory array (Lin, column 11, lines 20-36), Lin fails to disclose a **single status register** that provides status information of the first plane, the second plane, the third plane, and the fourth plane.

The Examiner also rejected claim 1 under 35 U.S.C. § 102(e) as being anticipated by Alexis. Applicants submit that claim 1 as amended is not anticipated under 35 U.S.C. § 102(b) by Alexis. Claim 1 includes the limitations:

> a memory array having a first plane, a second plane, a third plane, and a fourth plane, wherein a first partition of the memory array comprises one of the planes and a second partition of the memory array comprises the remaining planes, wherein a write operation is performed on the first partition and a read operation is concurrently performed on the second partition; and
>
> a status register coupled to the memory array, wherein the status register provides status information of the first plane, the second plane, the third plane, and the fourth plane.

(Amended claim 1) (emphasis added).

In contrast, Alexis discloses a flash memory 115 that includes a memory array 130 and status registers 150 (Alexis, column 4, lines 8-10). The memory array 130 includes a read plane 135 and a write plane 145 (Alexis, column 3, lines 9-12 and column 4, lines 51-53). The flash memory 115 also includes a status register for each of the first and second planes 135 and 140 of the

memory array 130 (Alexis, column 5, lines 24-26). Alexis does not disclose a memory array having a first plane, a second plane, a third plane and a fourth plane. Further, even if Alexis did disclose a memory comprising the first plane, the second plane, the third plane, and the fourth plane, Alexis fails to disclose a first partition that comprises one of the planes and a second partition that comprises the remaining planes.

Given that claims 2-5 depend from claim 1, applicants submit that claims 2-6 are not anticipated under § 102(b) or § 102(e) by the references cited by the Examiner.

Applicants submit that claim 6 as amended is not anticipated under 35 U.S.C. § 102(e) by Alexis. Claim 6 includes the limitations:

> dividing the memory array into n planes, wherein n is an integer greater than two;
> defining a write partition, wherein the write partition is a single plane of the memory array;
> defining a read partition, wherein the read partition is made up of all of the remaining n planes of the memory array; and
> providing the status of the read partition and the write partition of the memory array with a single status register.

(Amended claim 6) (emphasis added).

In contrast, Alexis discloses dividing a memory array 130 into first and second planes 135 and 140 (Alexis, column 4, lines 51-55). Alexis does not disclose dividing a memory array into n planes, wherein n is an integer greater than two. In addition, Alexis does not disclose defining a write partition, wherein the write partition is a single plane of the memory array and defining a read partition, wherein the read partition is made up of all of the remaining n planes of

the memory array (where n is greater than two).

Given that claims 7-11 depend from claim 6, applicants submit that claims 7-11 are not unpatentable under § 103(a) over the reference cited by the Examiner.

Applicants submit that claim 18 as amended is not anticipated under 35 U.S.C. § 102(b) by Line. Claim 18 includes the limitation:

> means for partitioning a memory array into a fixed first partition and a variable second partition to enable multiple operations to be performed on the memory array at the same time; and
> means for monitoring the operations performed on the memory array.

(Amended claim 18) (emphasis added).

In contrast, Lin discloses an array 10 having a fault tolerant section 11 and a header section 12 (Lin, column 4, lines 46-48). Lin does not disclose partitioning a memory array into a fixed first partition and a variable second partition as set forth in amended claim 18. Furthermore, even if Lin discloses partitioning a memory array into a fixed first partition and a variable second partition, Lin does not disclose enabling multiple operations to be performed on the memory array at the same time. Lin discloses a state machine 19 that includes resources for controlling the reading, programming, erasing and verifying of the array 10 (Lin, column 5, lines 40-43). The state machine 19 of Lin, however, does not enable the reading, programming, and verifying of data in the fault tolerant section 11 and the header section 12 at the same time.

Applicants submit that claim 18 as amended is not anticipated under 35 U.S.C. § 102(e) by Alexis. Claim 18 includes the limitation:

means for partitioning a memory array into a fixed first partition and a variable second partition to enable multiple operations to be performed on the memory array at the same time; and

means for monitoring the operations performed on the memory array.

(Amended claim 18) (emphasis added).

In contrast, Alexis discloses a means for partitioning a memory array 130 into first and second planes 135 and 140 (Alexis, column 4, lines 51-55). Alexis does not disclose partitioning a memory array into a fixed first partition and a variable second partition.

Given that claim 19 depends from claim 18, applicants submit that claim 19 is not anticipated under § 102(b) or § 102(e) by the references cited by the Examiner.

Respectfully submitted,
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